

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 1 1. (Currently amended) A method to facilitate cache coherence with
2 adaptive write updates, comprising:
3 initializing a cache to operate using a write-invalidate protocol;
4 monitoring a dynamic behavior of the cache during program execution,
5 wherein monitoring the dynamic behavior of the cache involves maintaining a
6 count for each cache line of the number of cache line invalidations the cache line
7 has been subject to during program execution; and
8 if the dynamic behavior indicates that better performance can be achieved
9 using a write-broadcast protocol, switching the cache to operate using the write-
10 broadcast protocol.
- 1 2. (Original) The method of claim 1, wherein monitoring the dynamic
2 behavior of the cache involves monitoring the dynamic behavior of the cache on a
3 cache-line by cache-line basis.
- 1 3. (Original) The method of claim 2, wherein switching to the write-
2 broadcast protocol involves switching to the write-broadcast protocol on a cache-
3 line by cache-line basis.
- 1 4 (Canceled).

1 | 5. (Currently amended) The method of ~~claim 4~~ claim 1, wherein if the
2 number of cache line invalidations indicates that a given cache line is updated
3 frequently, switching the cache line to operate under the write-broadcast protocol.

1 6. (Original) The method of claim 5, wherein if a given cache line is using
2 the write-broadcast protocol and the number of cache line updates indicates that
3 the given cache line is not being contended for by multiple processors, switching
4 the given cache line back to the write-invalidate protocol.

1 | 7. (Currently amended) The method of ~~claim 4~~ claim 1, wherein if a shared
2 memory multiprocessor includes modules that are not able to switch to the write-
3 broadcast protocol, the method further comprises locking the cache into the write-
4 invalidate protocol.

1 8. (Original) The method of claim 1, wherein the write-invalidate protocol
2 sends an invalidation message to other caches in a shared memory multiprocessor
3 when a given cache line is updated in a local cache.

1 9. (Previously presented) The method of claim 1, wherein the write-
2 broadcast protocol broadcasts an update to other caches in a shared memory
3 multiprocessor when the given cache line is updated in a local cache.

1 10. (Currently amended) An apparatus to facilitate cache coherence with
2 adaptive write updates, comprising:
3 an initializing mechanism configured to initialize a cache to a write-
4 invalidate protocol;
5 an monitoring mechanism configured to monitor a dynamic behavior of
6 | the cache, wherein monitoring the dynamic behavior of the cache involves

7 | maintaining a count of cache line invalidations initiated by each processor within
8 | a shared memory multiprocessor; and
9 | a protocol switching mechanism configured to switch the cache to a write-
10 | broadcast protocol if the dynamic behavior indicates that better performance can
11 | be achieved using the write-broadcast protocol.

1 | 11. (Original) The apparatus of claim 10, wherein monitoring the dynamic
2 | behavior of the cache involves monitoring the dynamic behavior of the cache on a
3 | cache-line by cache-line basis

1 | 12. (Original) The apparatus of claim 11, wherein switching to the write-
2 | broadcast protocol involves switching to the write-broadcast protocol on a cache-
3 | line by cache-line basis.

1 | 13 (Canceled).

1 | 14. (Currently amended) The apparatus of ~~claim 13~~ claim 10, wherein if
2 | the count of cache line invalidations indicates that a given cache line is updated
3 | frequently in different caches of the shared memory multiprocessor, switching the
4 | cache to the write-broadcast protocol.

1 | 15. (Original) The apparatus of claim 14, wherein if the given cache line is
2 | using the write-broadcast protocol and the count of cache line invalidations
3 | indicates that the given cache line is being invalidated in only one cache,
4 | switching the cache to the write-invalidate protocol.

1 | 16. (Currently amended) The apparatus of ~~claim 13~~ claim 10, further
2 | comprising a locking mechanism configured to lock the cache into the write-

3 invalidate protocol if the shared memory multiprocessor includes modules that are
4 not able to switch to the write-broadcast protocol.

1 17. (Original) The apparatus of claim 10, wherein the write-invalidate
2 protocol involves sending an invalidate message to other caches within a shared
3 memory multiprocessor when a given cache is written to.

1 18. (Original) The apparatus of claim 10, wherein the write-broadcast
2 protocol involves broadcasting a data update message to other caches within a
3 shared memory multiprocessor when a given cache is written to.

1 19. (Currently amended) A computing system that facilitates cache
2 coherence with adaptive write updates, comprising:
3 a plurality of processors, wherein a processor within the plurality of
4 processors includes a cache;
5 a shared memory;
6 a bus coupled between the plurality of processors and the shared memory,
7 wherein the bus transports addresses and data between the shared memory and the
8 plurality of processors
9 an initializing mechanism configured to initialize the cache to a write-
10 invalidate protocol;
11 a monitoring mechanism configured to monitor a dynamic behavior of the
12 cache, wherein monitoring the dynamic behavior of the cache involves
13 maintaining a count of cache line invalidations initiated by each processor within
14 a shared memory multiprocessor; and
15 a protocol switching mechanism configured to switch the cache to a write-
16 broadcast protocol if the dynamic behavior indicates that better performance can
17 be achieved using the write-broadcast protocol.

1 20. (Currently amended) A means to facilitate cache coherence with
2 adaptive write updates, comprising:
3 an initializing means for initializing a cache to a write-invalidate protocol;
4 a monitoring means for monitoring a dynamic behavior of the cache,
5 wherein monitoring the dynamic behavior of the cache involves monitoring the
6 dynamic behavior of the cache on a cache-line by cache-line basis; and
7 a protocol switching means for switching the cache to a write-broadcast
8 protocol if the dynamic behavior indicates that better performance can be
9 achieved using the write-broadcast protocol.